## AMENDMENT TO THE CLAIMS

The status of the claims of the present application stands as follows:

1. **(Canceled)**

2. **(Currently Amended)** An integrated circuit according to claim ~~1~~21, further comprising a scan clock tree electrically connected to said input.

3. **(Currently Amended)** An integrated circuit according to claim ~~1~~21, wherein said delay-compensation circuit comprises a pulse generator for generating a first clock pulse for said first latch.

4. **(Original)** An integrated circuit according to claim 3, wherein said pulse generator comprises an AND gate and an inverter.

5. **(Currently Amended)** An integrated circuit according to claim ~~1~~21, wherein said first clock signal comprises a plurality of first pulses each having a first duration and said second clock signal comprises a plurality of second pulses each having a second duration shorter than said first duration.

6. **(Original)** An integrated circuit according to claim 5, wherein each of said plurality of second pulses is generated substantially simultaneously with a corresponding one of said plurality of first pulses.

7. **(Canceled)**

8. **(Currently Amended)** An integrated circuit according to claim ~~7~~22, wherein said delay-compensation circuit element is an AND gate.

9. **(Original)** An integrated circuit according to claim 8, wherein said AND gate has a first input for receiving said first clock signal, a second input for receiving a third clock signal that is substantially the inverse of said first clock signal and a first output in electrical communication with said master latch, said first output for outputting said second clock signal.

10. **(Currently Amended)** An integrated circuit according to claim ~~7~~22, further comprising a multiplexer in electrical communication with said master latch.

11. **(Currently Amended)** An integrated circuit according to claim ~~7~~22, comprising at least one first scan chain comprising a plurality of first shift register latches.

12. **(Currently Amended)** An integrated circuit according to claim 11, further comprising at least one second scan chain comprising a plurality of second shift register latches, each of said plurality of second shift register latches lacking said delay-compensation circuit element.

13. **(Currently Amended)** An integrated circuit according to claim ~~7~~22, wherein said first clock tree is an LSSD scan clock tree.

14. **(Canceled)**

15. **(Currently Amended)** A device according to claim ~~1~~423, further comprising a scan clock tree electrically connected to said input.

16. **(Currently Amended)** A device according to claim ~~1~~423, wherein said delay-compensation circuit comprises a pulse generator for generating a first clock pulse for said first latch.

17. **(Original)** A device according to claim 16, wherein said pulse generator comprises an AND gate and an inverter.

18. **(Currently Amended)** A device according to claim ~~1~~423, wherein said first clock signal comprises a plurality of first pulses each having a first duration and said second clock signal comprises a plurality of second pulses each having a second duration shorter than said first duration.

19. **(Original)** A device according to claim 18, wherein each of said plurality of second pulses is generated substantially simultaneously with a corresponding one of said plurality of first pulses.

20. **(Currently Amended)** A device according to claim ~~14~~23, wherein said at least one shift register latch further comprises a multiplexer in electrical communication with said first latch.

21. (**New**) An integrated circuit, comprising:
    a) a first shift register latch responsive to a first clock signal;
    b) at least one second shift register latch responsive to said first clock signal, wherein said first clock signal at said at least one second shift register latch has a delay relative to said first clock signal at said first shift register, said at least one second shift register latch comprising:
        i) a first latch;
        ii) a second latch in electrical communication with said first latch;
        iii) an input for receiving said first clock signal; and
        iv) a delay-compensation circuit connected between said input and said first latch, said delay-compensation circuit configured to generate a second clock signal as a function of said first clock signal so as to compensate for said delay in said first clock signal.

22. (**New**) An integrated circuit, comprising:
    a) a first clock tree for receiving a first clock signal having a plurality of pulses each having a first width; and
    b) a first shift register latch responsive to said first clock signal;
    c) at least one second shift register latch responsive to said first clock signal, wherein said first clock signal at said at least one second shift register latch has a delay relative to said first clock signal at said first shift register, said at least one second shift register latch comprising:
        i) a master latch;
        ii) a slave latch in electrical communication with said master latch; and
        iii) a delay-compensation circuit element connected between said first clock tree and said master latch, said delay-compensation circuit element adapted for generating a second clock signal as a function of said first clock signal so as to compensates for said delay in said first clock signal.

23. **(New)** A device, comprising:

a) a power supply,

b) an integrated circuit electrically connected to said power supply, said integrated circuit including a first shift register latch responsive to a first clock signal and at least one second shift register latch responsive to said first clock signal, wherein said first clock signal at said at least one second shift register latch has a delay relative to said first clock signal at said first shift register, said at least one second shift register latch comprising:

i) a first latch;

ii) a second latch in electrical communication with said first latch;

iii) an input for receiving said first clock signal; and

iv) a delay-compensation circuit connected between said input and said first latch, said delay-compensation circuit configured to generate a second clock signal as a function of said first clock signal so as to compensate for said delay in said first clock signal.